Instabilities in Amorphous Oxide Semiconductor Thin-Film Transistors

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(Invited Paper)

***Abstract*—Thin-film transistors (TFTs) fabricated using amorphous oxide semiconductors (AOS) exhibit good electron mobility (5 to $> 50\ \mathrm{cm^2/V \cdot s}$), they are transparent, and they can be processed at low temperatures. These new materials show a great promise for high-performance large-area electronics applications such as flexible electronics, transparent electronics, and analog current drivers for organic light-emitting diode displays. Before any of these applications can be commercialized, however, a strong understanding of the stability and reliability of AOS TFTs is needed. The purpose of this paper is to provide a comprehensive review and summary of the recently emerging work on the stability and reliability of AOS TFTs with respect to illumination, bias stress, ambient effects, surface passivation, mechanical stress, and defects, as well as to point out areas for future work. An overview of the TFT operation and expected reliability concerns as well as a brief summary of the instabilities in the well-known Si_3N_4/a-Si:H system is also included.**

***Index Terms*—Amorphous oxide semiconductors (AOS), bias stressing, reliability, stability, transparent thin-film transistors (TTFTs).**

I. Introduction

ACTIVE matrix liquid crystal displays (AMLCDs) and other large-area electronics applications are currently dominated by thin-film transistors (TFTs) based on either amorphous or polycrystalline Si. Although hydrogenated amorphous Si (a-Si:H) allows fabrication of TFT arrays at low temperature and low cost and has been well proven for large-area commercial applications, this technology is plagued by low electron mobility ($\sim 1\ \mathrm{cm^2/V \cdot s}$) and well-known instabilities with respect to bias stressing [1] and light exposure [2]. Polycrystalline Si-based TFTs, on the other hand, can exhibit electron mobility in excess of $50\ \mathrm{cm^2/V \cdot s}$, but large-area applications have been proven to be difficult, and the relatively high thermal budget makes poly-Si unsuitable for flexible substrates. In addition, both of these materials are opaque, which is a disadvantage for display applications. Thus, the search has continued for higher mobility materials that allow for a stable device operation and that can be processed at low temperatures.

In 2003, several groups reported on transparent TFTs (TTFTs) based on ZnO, which is a wide-bandgap semiconductor [3]–[5]. These original devices generated excitement not only because they were transparent but also because they exhibited electron mobilities (μ) of 0.3–2.5 $\mathrm{cm^2/V \cdot s}$, threshold voltages (V_T) as low as ~0–3 V [4], [5], and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratios of $\sim 10^7$. Since this original ZnO work, a number of novel materials have been used to make TFTs and TTFTs, including In_2O_3, SnO_2, InGaZnO (IGZO), ZnSnO (ZTO), ZnInO (ZIO), SnGaZnO (TGZO), InGaO (IGO), ZnInSnO (ZITO), and ZnON. All of these materials are n-type due to the existence of intrinsic donors. Although ZnO, In_2O_3, and SnO_2 are typically polycrystalline in thin-film form, crystallization is frustrated in multicomponent materials such as IGZO, ZTO, ZIO, IGO, TGZO, and ZITO. These latter materials are referred to as amorphous oxide semiconductors (AOS).

This relatively new class of materials possesses several advantages for TFT applications [6], which include the following: 1) an amorphous crystal structure which, due to a lack of grain boundaries, can aid in achieving good uniformity and relatively easier manufacturing; 2) low-temperature processing, which is suitable for flexible substrates such as plastic or Mylar; 3) electron mobility in the range of 5 to $> 50\ \mathrm{cm^2/V \cdot s}$, which is about ten times greater than a-Si:H; 4) low sensitivity to visible light; and 5) transparency in visible region.

A unique aspect of these AOS materials is that the electron mobility is not strongly sensitive to the crystal structure, as is the case for Si or other covalently bonded semiconductors. The low sensitivity of the AOS mobility to the crystal structure was explained by Nomura *et al.* [7] as arising from the nature of the chemical bonding in these $(n-1)\mathrm{d}^{10}\mathrm{ns}^0$ $(n \geq 4)$ metal oxides. Carrier transport in covalently bonded materials such as Si is primarily through the directional sp^3 orbitals so that introducing randomness into the structure greatly reduces bond overlap and carrier mobility. In $(n-1)\mathrm{d}^{10}\mathrm{ns}^0 (n \geq 4)$ metal oxides, the higher ionicity of the bonding leads to a conduction band based on nondirectional ns orbitals. Because the overlap of these s orbitals is not significantly altered by the introduction of randomness, carrier transport and, thus, mobility is relatively insensitive to randomness. Therefore, although the mobility of amorphous Si is more than two orders of magnitude less than that of polycrystalline Si, the mobility of the AOS materials is only about two to five times less than their crystalline

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counterparts. This fundamental difference in bonding may also play a role in TFT stability and reliability [8], [9].

Although it will be extremely difficult to displace a-Si:H in the mature AMLCD industry, AOS materials offer great promise for the upcoming and potential applications such as TFT backplanes for high-performance AMLCDs, 3-D displays, active matrix organic light-emitting diode (AMOLED) displays, flexible electronics, and transparent electronics [6], [10]–[14]. For example, it is thought that future high-end products, such as ultrahigh-resolution displays with frame rates greater than 120 Hz and sizes greater than 50 in, will require transistors with higher performance than a-Si:H [10], [13], [14]. The AOS TFTs may also be a viable option for AMOLEDs. Because AMOLED displays are emissive and current driven, TFT stability is critical. Although mobility and threshold voltage (V_t) stability are typically not vitally important for a switching transistor, the brightness of each pixel in an emissive AMOLED display is highly dependent on the drain current of the driving transistor [13]–[15]. TFTs must remain stable over time as any shift in V_T would change the brightness of an individual pixel and would cause display nonuniformity [6], [13]–[18]. Although it is possible to use a-Si:H for this application, its inherent instabilities must be compensated with additional TFTs, resulting in a substantial area penalty and a reduction in the "transparency" of the display [11].

Despite the importance of a stable operation for potential applications, there have been relatively few studies to date on the stability and reliability of the many new AOS TFTs. However, even though this work is still at an early stage, a number of potential reliability problems have been identified and have begun to be characterized in a number of systems. The purpose of this paper is to provide a comprehensive review and summary of the rapidly expanding work on instabilities in AOS TFTs and TTFTs caused by illumination, bias stress, ambient/surface interaction, simultaneous light exposure/bias stressing, and mechanical stress, as well as the impact of surface passivation and the current understanding of defects. Areas for future work are identified. A brief background discussion of TFT structure, TFT operation, and types of instabilities is included to aid the reader in interpreting this work. To help place this emerging AOS work in perspective, brief summaries of the well-known instabilities in the Si_3N_4/a-Si:H system are also included. Note that this review will focus on the stress-induced changes in performance rather than the overall electrical performance (see [6]), and thus, it will primarily include studies with stability and reliability results.

II. TFT Background

To provide a basis for understanding and interpreting the recent work that is investigating the stability and reliability of new AOS TFTs and TTFTs, a brief discussion of TFT structure, operation, and potential instability problems is included in this section.

A. TFT and TTFT Device Structure

There are four major classes of TFT devices: 1) staggered top gate; 2) staggered bottom gate (SBG); 3) coplanar top gate;

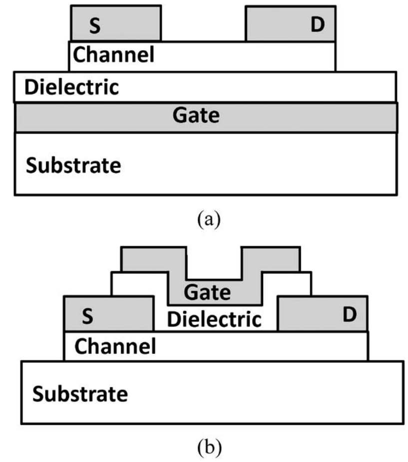

Fig. 1. Schematic cross section of the (a) SBG and (b) coplanar top gate TFTs.

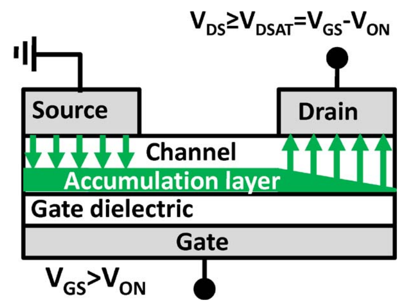

Fig. 2. Schematic cross section of an SBG TFT operating in accumulation (adapted from the study in [6]).

and 4) coplanar bottom gate [19]. For the AOS work published to date, the SBG structure dominates with only a few groups fabricating coplanar top gate devices. Shown in Fig. 1 are schematic cross sections of the (a) SBG and (b) coplanar top gate structures. In the SBG device structure [Fig. 1(a)], the gate electrode is deposited first, followed by the gate dielectric, the AOS channel, and finally the source and the drain. When we say staggered, it is meant that the source and the drain are not in the same plane as the conductive channel. The gate electrode can be either a blanket film or a patterned film. For TTFTs, the substrate is typically glass, and a transparent conductor such as ITO or ZnO:Al is used for the source, gate, and drain.

B. TFT Operation

All of the new AOS materials listed in the introduction are intrinsically n-type. A major challenge for the oxide semiconductor technology has been the formation of p-type material [20]. Because only the n-type material is available, operation differs from that of the MOS technology in which the device is turned on by the formation of an inversion layer. For disordered wide-bandgap AOS TFTs, inversion is not practical, and devices must be operated in accumulation [6], [21]. As shown in Fig. 2, the AOS TFTs are turned on by applying a positive bias to the gate in order to form an accumulation layer in the AOS channel. As in a MOS device, pinchoff and saturation occur when $V_{DS} > (V_G - V_{ON})$. Note that, in the SBG configuration shown, electron transport takes place from the source, across the thickness of the AOS layer to the

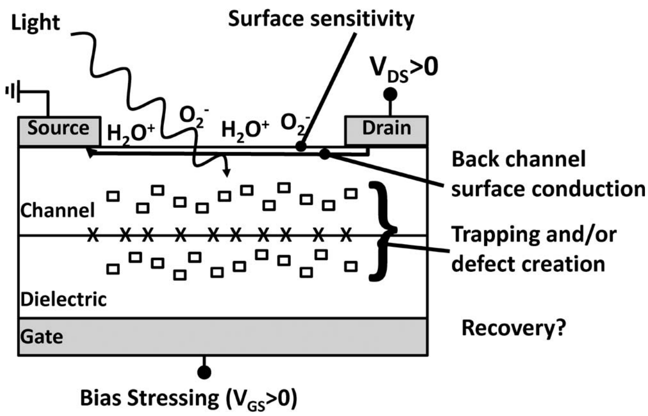

Fig. 3. Schematic summary of the potential instabilities in the AOS TFTs.

AOS/gate dielectric interface, along this interface, and then back across the thickness of the AOS layer to the drain. Note also that the carrier density in the AOS channel layer must be low (typically $10^{13}-10^{16}/\mathrm{cm}^3$) or the device functions as a voltage-controlled resistor rather than as a transistor. As AOS TFTs are being considered for macroelectronics applications, the majority of the reported devices are typically very large compared to MOSFETs, with lengths and widths typically in the range of 10s to greater than 100 μm.

C. Stability Concerns in the AOS TFTs

Based on the understanding that has been developed for a-Si:H/Si_3N_4 TFTs [1], [2], [19], the following can be expected: 1) light exposure/illumination and 2) bias stressing may lead to instabilities such as charge trapping and, possibly, defect formation in the AOS, in the gate dielectric, or at the AOS/dielectric interface. It might also be expected that an increased temperature or a simultaneous exposure of a device to both bias stress and illumination could lead to enhanced or additional instabilities. In the SBG structure shown in Fig. 1(a), the AOS surface is exposed to ambient. Metal oxides are well known as gas sensors [22]–[25], and thus, one might also expect instabilities due to 3) AOS surface/ambient interaction. While not an issue for top-gate configurations, the interaction with ambient molecules on the AOS surface could lead to "back-channel" surface conduction in the bottom gate devices. The encapsulation or passivation of the AOS surface, so as to reduce or eliminate the interaction with the ambient, would be expected to have an impact on the operation and stability of bottom gate devices. Finally, the generation and recovery of all of these instabilities over time may lead to a time-dependent operation. The stability concerns are shown in Fig. 3.

III. Review of the AOS TFT Stability Studies

In this section, recently emerging work concerning the stability of TFTs made from a variety of AOS materials in various device configurations will be reviewed. In particular, illumination, bias stressing, and surface-related instabilities will be discussed. The interactions between these (such as simultaneous illumination/bias stressing) as well as the impact of passivation will also be discussed. To help put these results in context, brief summaries of the response of the a-Si:H TFT technology are included.

A. Illumination

In a commercial AMLCD, switching TFTs are continuously exposed to illumination from the backlight [10]. Thus, for AMLCD as well as transparent applications, TTFTs should be insensitive to visible light. Staebler and Wronski [2] were the first to demonstrate that a-Si:H suffers degradation under illumination (the well-known Staebler–Wronski Effect). For example, efficiency of a-Si:H solar cells is reduced after initial exposure to light. They reported a permanent increase in defect density during illumination, which was reversible, but required annealing at $\sim$180 °C$-$200 °C. Note that, although wide-bandgap devices might be expected to be unaffected by subbandgap illumination, the presence of bandtail states in these amorphous materials can lead to bandgap narrowing and absorption at longer wavelengths [21], [26]. This section discusses recent reports of the impact of various wavelength illumination on a variety of unbiased and unpassivated TFTs.

Gorrn *et al.* [27] looked at 628–425-nm illumination of unencapsulated SBG ZTO TFTs with 220-nm ATO gate dielectrics. ATO is an aluminum oxide/titanium oxide laminate deposited via atomic layer deposition (ALD) at 350 °C. A 60-nm ZTO channel with a Zn-to-Sn composition ratio of 36:64 was then deposited via plasma assisted pulsed laser deposition (PA-PLD) at 450 °C. They reported a little change as a result of the 628-nm illumination. Illumination at 425, 470, and 525 nm, however, resulted in a decrease in V_T and μ_{sat} and an increase in $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$, with the parameter shift occurring over a period of hours. A shorter λ and a higher intensity resulted in greater parametric shifts. The magnitude of these shifts was strongly dependent on the ZTO deposition temperature. The samples deposited at 250 °C showed a 20% decrease in μ_{sat}, while the samples deposited at 350 °C and above showed less than 20% shift. All light-induced changes were found to be fully reversible, and they recovered to the initial values when the light was turned off. Persistent photoconductivity was observed with an $\sim$20-h time constant. They concluded that the time constant of the recovery was not governed by the dielectric, but they suggested that the persistent photoconductivity may be due to temporary trapping or, since these devices were unpassivated, oxygen readsorption at the surface. Shown in Fig. 4 is a plot of V_T and the saturation mobility (μ_{SAT}) versus time during and after exposure to a 425-nm light. During illumination, V_T shifts negatively, and μ_{SAT} is reduced. After the exposure ends, both V_T and μ_{SAT} recover over a period of many hours. They later determined that chemisorption of oxygen is critical concern for stability [70].

Paine *et al.* [28] examined unpassivated SBG IZO TTFTs, with the SiO_x gate dielectric deposited via plasma-enhanced chemical vapor deposition (PECVD) at 280 °C and with the IZO channel dc sputtered at room temperature. Similar to the study in [27], they found out that, while ambient fluorescent light exposure produced little effect, devices exposed to UV illumination showed the time-dependent increase in conductivity and decrease in $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$. The full recovery of the persistent photoconductivity occurred over a period of 24 h.

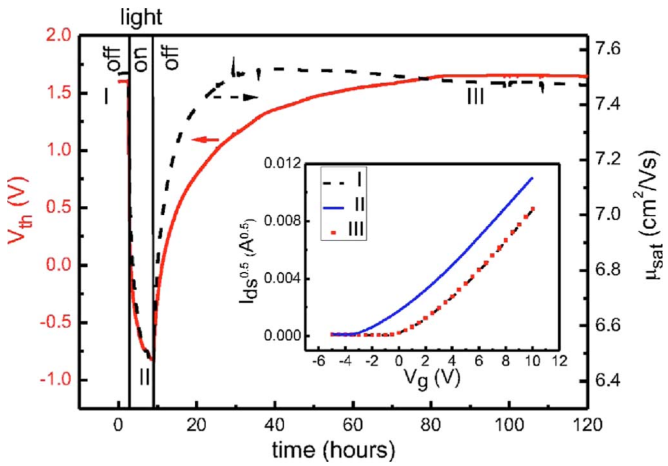

Fig. 4. Data from the study in [27]. Plot of (solid red) V_T and (dashed black) μ_{sat} versus time during and after a 425-nm illumination. The inset shows the I_D versus V_G transfer curves. I—(Dashed black) Preillumination. II–(Solid blue) During illumination. III–(Dotted red) After full recovery.

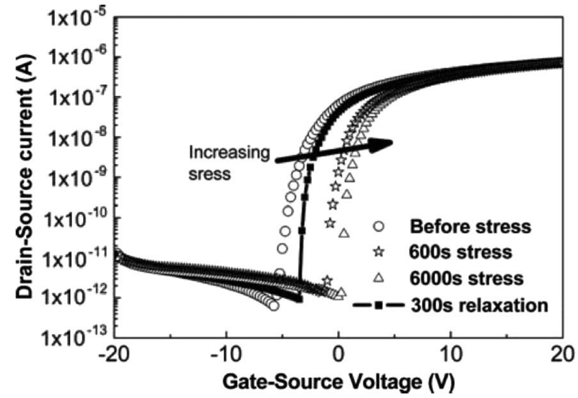

Fig. 5. Data from the study in [31]. Transfer characteristics for an SBG In_2O_3 TFT, with the 200-nm PECVD SiO_x gate dielectric and the 100-nm In_2O_3 channel deposited via reactive ion beam assisted evaporation, measured (circles) before stress, (stars) after a 600-s stress (with $V_G = V_{DS} = +10$ V), (triangles) after a 6000-s stress, and (solid) after a 300-s relaxation.

Barquinha *et al.* [29] also reported similar results for unpassivated SBG IZO TTFTs, with the 220-nm ATO gate dielectric deposited via ALD at 350 °C and with the 80-nm IZO channel deposited via room temperature RF sputtering. Visible to UV illumination produced a decrease in $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ and mobility, a negative shift of V_{ON}, and an increase in hysteresis.

In summary, it has generally been reported that, for unbiased devices, longer wavelength ambient lighting, well below the bandgap, has little effect [27]–[29]. For shorter wavelength exposures approaching the bandgap, V_{ON} shifts negatively, ΔV_{HYS} increases, $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ decreases, mobility (μ) decreases, and subthreshold swing (S) increases as λ decreases. Higher intensity light and longer exposure times typically result in a greater parametric shift. In contrast to a-Si:H, all of these effects appear to be reversible when left in the dark at room temperature. Note that it is likely that at least some of the illumination-induced effects that have been reported could be attributed to the interaction of the light with the ambient gas molecules on the unpassivated AOS channel surface rather than to the direct interaction of the light with the AOS material (see Section III-C). Note that wavelengths below 430 nm may be filtered without compromising display performance [27]. The effect of illumination during bias stressing is discussed in the following section.

B. Bias Stressing

Bias stressing of a-Si:H/Si_3N_4 TFTs results in the following two primary instability mechanisms [1], [19]: 1) defect creation in the channel and 2) trapping in the gate dielectric or at the dielectric/channel interface. Although these effects can be recovered by elevated temperature annealing, they are irreversible without annealing.

Very recently, a number of gate bias and combined gate/drain bias (bias-current) stressing studies have been conducted on various AOS/dielectric TFT combinations. These studies will be subdivided into low-field positive gate bias stressing, high-field positive gate bias stressing, negative gate bias stressing, dynamic bias stressing, bias stressing under illumination, and process dependence. For AMLCD applications, the transistor is not always on, and recovery when unbiased must be considered as well. This section will conclude with a discussion on modeling and potential mechanisms. Note that the focus will be on qualitative response. Due to differences in channel dimensions, stress conditions, device structure, passivation, etc., it is not simple to compare precisely quantitative responses to stressing.

1) Low-Field Positive Gate Bias Stressing: Many groups have investigated the impact of low-field ($\lesssim 1$ MV/cm) positive bias stressing on a variety of different material systems [30]–[50]. The AOS materials investigated include ZnO, ZTO, and In_2O_3, with the majority of the work being performed on IGZO. The dielectric materials include SiO_2, Al_2O_3, ATO, and SiN_x. Unless otherwise noted, devices may be assumed to be *without* surface passivation. As discussed in Section III-D and E, ambient and surface passivation can have a large impact on bias stressing. The devices discussed in this section may be assumed to have been stressed in air, at room temperature, and in the dark, unless otherwise indicated. Bias stressing during illumination is also discussed in the following discussion.

The first bias stressing study of oxide semiconductor TFTs was performed by Cross and DeSouza on SBG ZnO TFTs consisting of an RF-magnetron-sputtered 100-nm ZnO channel on a 150-nm thermally grown SiO_2 gate dielectric [30]. In this paper, they reported that stressing for up to 10^4 s at a V_G of up to +30 V produced a positive parallel V_T (or V_{ON}) shift, with little or no change in S or μ. A rapid recovery was observed without annealing or bias. Similar results have been reported in a variety of other SBG TFT and TTFT systems. Representative low-field stressing results from Vygraneko *et al.* [31] are shown in Fig. 5.

Other material systems in which a similar response to low-field stressing was reported include a 100-nm thermal SiO_2 gate dielectric/40-nm RF-sputtered amorphous IGZO channel SBG TFTs stressed with $V_G = +15$ V for up to 10^5 s [32], a 90-nm PECVD SiO_x gate dielectric/50-nm RF-sputtered amorphous IGZO channel SBG TFTs stressed at $V_G = +6$ V for 500 h [33], a 400-nm PECVD SiN_x gate dielectric/70-nm RF-sputtered amorphous IGZO (with SiO_x top surface passivation)

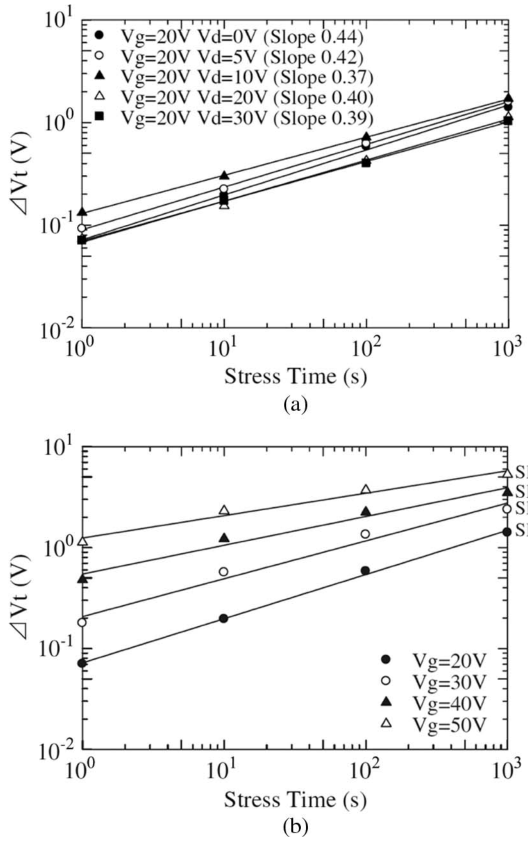

Fig. 6. Data from the study in [34]. ΔV_t versus stress time for a 400-nm PECVD SiN_x/70-nm RF-sputtered IGZO SBG TFTs with SiO_x top surface passivation (a) for various V_G/V_{DS} combinations and (b) as a function of the V_G stress voltage.

SBG TFTs stressed at a V_G of up to +50 V [34], a 120-nm thermally grown SiO_2/20-nm spin coated ZTO channel SBG TFTs stressed at $V_G = +20$ V for 3600 s [35], a 220-nm ALD ATO gate dielectric/60-nm PA-PLD amorphous ZTO (36% Zn/64% Sn) channel SBG TTFTs stressed at $V_G = +10$ V for up to 10^5 s [36], a 200-nm PECVD SiO_x gate dielectric/100-nm reactive ion beam assisted evaporation In_2O_3 channel stressed at $V_G = +10$ V for up to 6000 s [37], and a 300-nm Si_3N_4 gate dielectric/50-nm RF-magnetron-sputtered IZO coplanar bottom gate TFTs stressed at $V_G = +30$ V for up to 1.2×10^4 s [38].

As shown in Fig. 6, Fujii *et al.* [34] investigated low-field bias-current stressing with $V_G = +20$ V and a V_{DS} of up to +30 V and showed that the overall degradation mode was not changed by increasing V_{DS}. They still observed recoverable positive V_T shift, accompanied by little degradation of S and μ.

Other groups have also reported similar results to Fujii *et al.* for a combined positive-bias-current stressing $(V_G > 0; V_{DS} > 0 \text{ V})$ of various gate dielectric/AOS channel stacks, including a 220-nm ALD ATO gate dielectric/PLD amorphous IGZO SBG TTFTs stressed at $V_G = +30$ V and $V_{DS} = +1$ V [39]; a 150-nm thermal SiO_2/40-nm PLD amorphous IGZO channel SBG TFTs stressed at a constant current of $I_D = 5\ \mu$A, with $V_G = V_{DS}$, for 50 h [40]; a 100-nm thermal SiO_2/50-nm RF-sputtered amorphous IGZO channel SBG TFTs stressed at $V_G = V_{DS} = +30$ V for up to 10^5 s [41]; a 220-nm ALD ATO/60-nm PA-PLD ZTO (36% Zn/64% Sn) SBG TTFTs stressed at $V_G = V_{DS} = +10$ V, with $I_D = 188\ \mu$A [35], [42]; a 200-nm ALD Al_2O_3/RF-sputtered ZTO channel SBG TFTs stressed with $V_G = 20$ V and $V_{DS} = 1$ V [43]; a 200-nm RF-sputtered Al_2O_3 gate dielectric/60-nm RF-sputtered ZnO channel SBG TFTs stressed at $V_G = V_{DS} = +7$ V [44]; a 100-nm thermal SiO_2 gate dielectric/40-nm RF-sputtered IGZO channel SBG TFTs stressed at $V_G = +10$ V and $V_{DS} = +0.5$ V [18]; and 50-nm ZIO SBG TFTs with either 200-nm PECVD SiO_x or 200-nm PECVD SiN_x gate dielectrics stressed at $V_G = +20$ V and $V_{DS} = +0.1$ V [45]. Lee *et al.* [46] reported a similar response for organic photoacryl passivated IGZO SBG TFTs on flexible polyimide films with either 200-nm PECVD SiO_x or 200-nm PECVD SiN_x gate dielectrics stressed at $V_G = +15$ V and $V_{DS} = +5.1$ V, with the SiO_x gate dielectric devices exhibiting a reduced shift, possibly due to a reduced H content. In addition, the 200-nm PECVD SiO_x gate dielectric/amorphous IGZO channel coplanar homojunction bottom gate TFTs, with the PECVD SiO_x/Si_3N_4 (50/300 nm) surface passivation stressed at $V_G = V_{DS} = +12$ V and $I_D = 4\ \mu$A at 60 °C for 10^5 s, showed a small parallel positive V_T shift [47]. Zhao *et al.* [48] looked at the 50-nm Al_2O_3 gate dielectric/30-nm ZnO channel SBG TFTs that were surface passivated with a 30-nm layer of ALD Al_2O_3. Al_2O_3 gate dielectric and ZnO were deposited via a novel plasma-enhanced ALD process using either DEZ/N_2O or TMA/CO_2 as precursors. Low-field stressing at $V_G = V_D = +3$ V for 40 000 s resulted in a very small (< 50 mV) V_T shift. Similar results were reported by Mourey *et al.* [49].

Although the vast majority of the groups have reported that a low-field positive bias stress results in a positive V_T shift, with little or no change in S or μ, there have been exceptions. Flewitt *et al.* [50] reported an increase in mobility in stressed thermal SiO_2/sputtered IZO SBG TFTs, which they attributed to a reduced trapping/detrapping in the IZO channel due to an increased occupancy of defects near the IZO conduction band under a positive gate bias. Although their similar devices with either PECVD SiO_x or SiN_x gate dielectrics exhibited a typical behavior (discussed earlier), Hoffman *et al.* [45] reported that the 50-nm ZIO channel SBG TFTs, with the HfO_2 gate dielectrics deposited by either ALD or sputtering, exhibited a complex response to low-field positive bias stressing. An initial positive V_T shift at short stress times was followed by a turnaround and increasing negative V_T shifts at longer stress times, which they did not attempt to explain.

To summarize, based on the observations of a rigid positive shift of V_T or V_{ON}, which is accompanied by little or no change in S or μ that is fully recoverable at room temperature, it has been generally concluded that electron trapping at or near the interface without the creation of new defects is the primary mechanism responsible for low-field stress-induced instabilities in AOS TFT devices.

Differences in the low-field bias stress response may be attributed to many things, including not only the details of the specific dielectric/channel interface [45], [46], [51], deposition methods, and postdeposition annealing but also bias-enhanced interaction between the ambient and the AOS surface in unpassivated devices. It is likely that in many of the early studies of unpassivated devices, the uncontrolled interaction with the ambient may have played a role in or may have even dominated the observed response (see Section III-C–E).

2) High-Field Positive Gate Bias Stressing: The reports on accelerated positive bias stressing of AOS TFTs at fields higher than 1 MV/cm are not as consistent as the reports on low-field stressing ($\lesssim$ 1 MV/cm). Again, unless otherwise noted, the devices are assumed to be stressed at room temperature in the dark *without* surface passivation.

Several groups have reported that high-field positive bias stressing ($>$ 1 MV/cm) is similar to low-field stressing ($\lesssim$ 1 MV/cm), with larger positive V_T shifts as the stress voltage is increased and with little or no change in S, μ, or $I_{\rm ON}/I_{\rm OFF}$ [39], [52], [53]. For example, Lim *et al.* [53] looked at 96-nm ALD Al_2O_3 gate dielectric/66-nm ZnO:N channel SBG TFTs in which the ZnO:N channel was deposited by a novel ALD process using DEZ/NH_4OH in H_2O as precursors. Positive bias stressing at $V_G = +15$ V and $V_{\rm DS} = +1$ V induced positive V_T shifts, with little change in S.

In other cases, high-field stressing ($\gtrsim$ 1 MV/cm) has been reported to lead to a recoverable S and/or μ degradation. In the first study of bias stressing of the unpassivated ZnO SBG TFTs, Cross and Desouza [30], [54] reported an increased S in thermal SiO_2 gate dielectric/RF-sputtered ZnO channel SBG TFTs stressed at $V_G \simeq +3$ MV/cm. In one of the few studies involving top gate devices, Lee *et al.* [55] saw that S degradation as result of $\sim +3$-MV/cm bias stress was worse when 5-nm PECVD SiN_x interfacial layer was inserted between the 185-nm ALD Al_2O_3 gate and the RF-sputtered IGZO channel layer. Both of these groups implicated trap creation at the interface.

Fung *et al.* [56] subjected the 100-nm RF-sputtered SiO_2/30-nm RF-sputtered IGZO channel SBG TFTs with sputtered SiO_2 channel encapsulation to an elevated temperature (40–80 °C) stress at $V_G = +14-20$ V and $V_{\rm DS} = 0$ V for up to 10^4 s and found a small fairly rigid positive V_T shift, with a slight increase in S and decrease in μ. Although they saw little recovery at room temperature, complete recovery was observed after a 2-h 200-°C anneal in air. They implicated carrier injection from the channel and subsequent charge trapping with little creation of new defects.

Overall, there are not as clear general trends for accelerated positive bias stressing at fields $>$ 1 MV/cm as there are for lower fields ($\lesssim$ 1 MV/cm). In addition to the degradation that is consistent with that widely reported at low fields (recoverable positive V_T shifts with no degradation of S and μ and charge trapping without defect creation), there are also reports on changes in S and μ, V_T shifts that require annealing, and defect creation. Besides material and processing differences, a likely explanation for the reduced agreement among high-field stressing studies is that surface/ambient interactions (see Section III-C–E) in unpassivated devices become even more important at higher fields.

3) Negative Gate Bias Stressing: n-type AOS TFTs operate in accumulation mode and require a positive gate bias to turn on. However, according to the study in [10], the amount of time that a typical TFT spends under a negative gate bias in AMLCD applications is approximately 500× the amount of time spent under a positive gate bias. Negative bias stress is therefore arguably as important or even more important than positive bias stress.

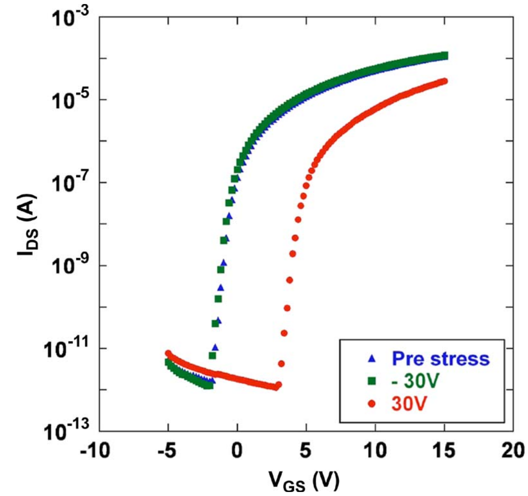

Fig. 7. Data from the study in [39]. Plot of I_D versus V_G for the 220-nm ATO/IGZO TTFTs stressed for 500 s under positive and negative gate biases, with $V_{\rm DS} = 1$ V.

Negative gate bias stressing is often reported to result in negligible changes in V_T, S, and μ when the devices are stressed in the dark (Unless otherwise noted, the devices are assumed to be stressed at room temperature and *without* surface passivation.). For example, as shown in Fig. 7, Suresh *et al.* [39] saw negligible changes in 220-nm ALD ATO gate dielectric/pulse laser deposited (PLD) IGZO channel SBG TTFTs stressed under a negative bias. Similar results were reported in other systems, including thermal SiO_2/RF-sputtered IGZO SBG TFTs [32], thermal SiO_2/spin coated ZTO SBG TFTs [35], and unilluminated PE-ALD Al_2O_3 dielectric/PE-ALD ZnO SBG TTFTs [57].

In other cases, negative bias stressing has been reported to result in degradation. Cross and DeSouza [54] reported a recoverable negative V_T shift in thermal SiO_2/RF-sputtered ZnO TFTs but concluded that their devices were "inherently unstable."

Gornn *et al.* [27] reported a negative V_T shift, with S degradation for ALD ATO dielectric/ZTO SBG TFTs but only for some compositions of ZTO. Liu *et al.* [38] subjected 300-nm Si_3N_4 gate dielectric/50-nm RF-magnetron-sputtered IZO coplanar bottom gate TFTs to $V_G = -30$ V for up to 1.2×10^4 s and saw negative V_T shifts, with little or no change in S and mobility. A nearly complete recovery was observed after 15 h at room temperature. Negative V_T shifts were also seen in PECVD SiO_x passivated IGZO SBG TFTs, with the 200-nm PECVD SiO_x gate dielectrics stressed at $V_G = -30$ V and $V_D = 10.1$ V [12].

Lee *et al.* [10] subjected SiN_x dielectric/IGZO SBG TFTs to negative bias current stressing with $V_G = -20$ V and $V_{\rm DS} = +10$ V at 60 °C while under illumination from a halogen lamp. As shown in Fig. 8, they reported a rigid negative shift, with insignificant changes in S and $\mu_{\rm FE}$. They observed similar results in the dark, but with a smaller magnitude of the V_T shift (Further discussion of bias stress under illumination appears in a following subsection.)

Seo *et al.* [58] subjected 200-nm PECVD SiN_x/60-nm a-IGZO channel SBG TFTs with and without TiO_x encapsulation to $V_G = -20$ V and $V_{\rm DS} = 0.1$ V for 3000 s

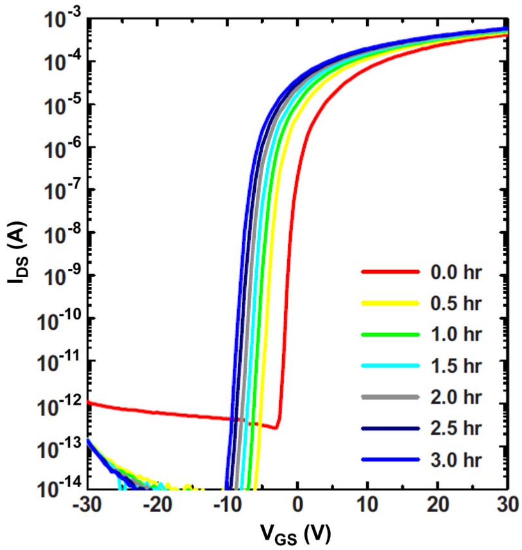

Fig. 8. Data from the study in [10]. Plot of I_D versus V_G as a function of time for the SiN_x dielectric/IGZO SBG TFTs exposed to a negative gate bias stress while under illumination.

at 60 °C and saw a rigid negative V_T shift, with no change in S and μ.

Fung *et al.* [56] subjected 100-nm RF-sputtered SiO_2/30-nm RF-sputtered IGZO channel SBG TFTs with sputtered SiO_2 encapsulation to an elevated temperature (40–80 °C) stress at $V_G = -12- -20$ V and $V_{DS} = 0$ V for up to 10^4 s and found a small fairly rigid negative V_T shift, with a slight increase in S and μ. Although they saw a little recovery at room temperature, complete recovery was observed after a 2-h 200-°C anneal in air. Lee *et al.*, Seo *et al.*, and Fung *et al.* all attributed the negative bias stress response to charge trapping at existing defects rather than to defect creation.

Finally, a *positive* V_T shift without recovery was reported in the 200-nm PECVD SiO_x/reactive ion beam assisted 30-nm In_2O_3 SBG TFTs stressed at $V_G = -30$ V [37].

In summary, the investigations of negative bias stressing appear to be divided between the following reports: 1) little effect and 2) negative V_T shift, with little degradation of S and μ. Besides material differences, recent reports stating that both illumination [57] and humidity [10] exacerbate the effects of negative bias stress may provide a partial explanation for the varying observations. Processing and encapsulation have also been shown to have an impact on negative bias stressing [27], [58]. These interactions are discussed further in the following sections.

4) Dynamic Stressing: It is known that static stress may be pessimistic for many applications [59] and therefore it is useful to assess device stability under dynamic stressing as well as static stressing. So far, the only study of the frequency dependence of the dynamic bias stressing of AOS TFTs was performed by Cho *et al.* [52] who subjected 100-nm thermal SiO_2 gate/40-nm RF-sputtered IGZO SBG TFTs to alternating cycles of stress ($V_G = +15$ V and $V_{DS} = 0$ V) and relaxation ($V_G = 0$ V and $V_{DS} = +15$ V). They found out that a positive gate bias dynamic stress results in positive V_T shifts with no S degradation that do not completely recover at room temperature. As shown in Fig. 9, they found out that

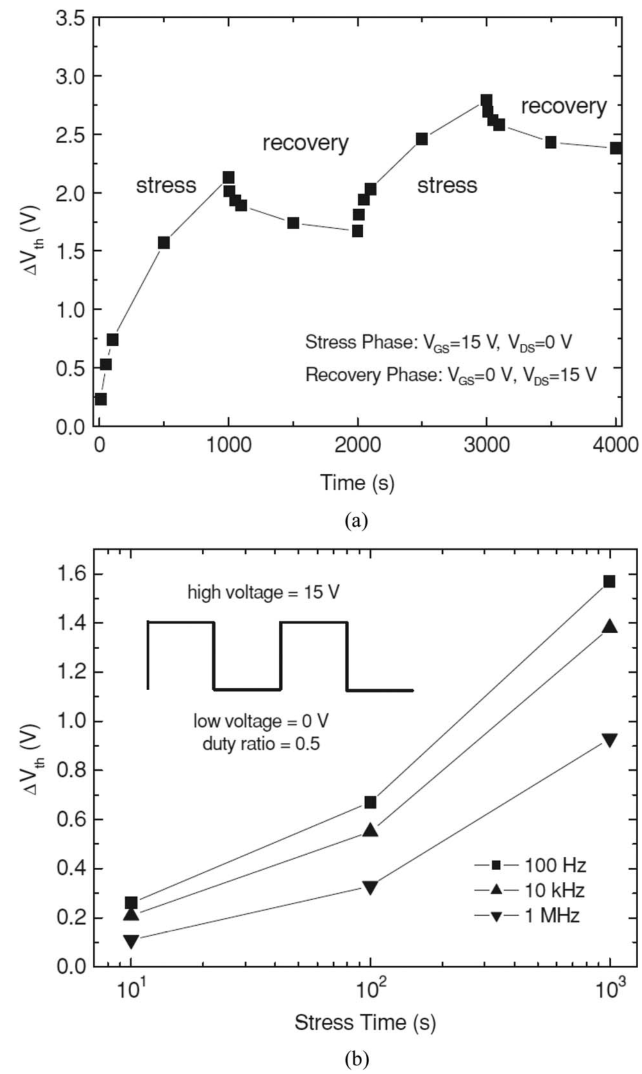

Fig. 9. Data from the study in [52]. Plot of ΔV_T versus time for 100-nm thermal SiO_2 gate/40-nm RF-sputtered IGZO channel SBG TFTs subjected to (a) alternating stress and recovery and (b) dynamic stress at several different frequencies.

higher frequency stressing results in less damage. The work of Cho *et al.* [52] emphasizes the need to understand both time-dependent stress and recovery effects with respect to the intended application.

5) Bias Stressing Under Simultaneous Illumination: In commercial AMLCD devices, switching TFTs are continuously exposed to illumination from the backlight [10]. Therefore, it is necessary not only to look separately at the impact of illumination and bias stressing on device operation but also to understand the impact of bias stressing while under continuous illumination. So far, it has been reported that illumination during bias stressing leads to an enhanced degradation.

Shin *et al.* [57] were the first to look at the impact of illumination on bias stressing. As shown in Fig. 10, for PE-ALD Al_2O_3/PE-ALD ZnO TFTs, they found out that a 524-nm illumination exacerbates the V_T shift for negative gate bias stressing but does not seem to impact positive gate bias stressing. Similar results were reported by Lee *et al.* [10] for SiN_x dielectric/IGZO SBG TFTs subjected to halogen lamp

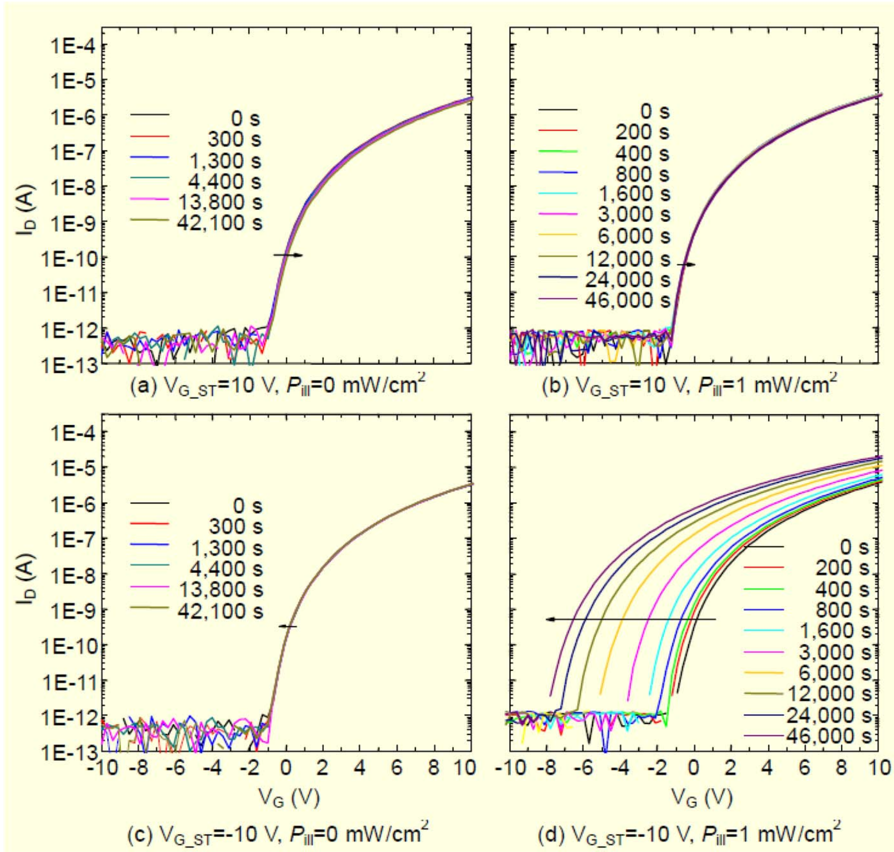

Fig. 10. Data from the study in [57]. Plot of I_D versus V_G for the PE-ALD Al_2O_3/PE-ALD ZnO TFTs exposed to either (a) and (b) positive or (c) and (d) negative V_G stress and either (b) and (c) under simultaneous exposure to 540-nm illumination or (a) and (c) in the dark.

illumination during negative gate bias stressing at an elevated temperature. They proposed that the main mechanism for the illumination-enhanced damage is the trapping of the photogenerated holes in the gate insulator and/or at the insulator/channel interface.

6) Process Dependence of Bias Stressing: Despite the broad qualitative similarities in low-field gate bias stressing response reported for a wide variety of AOS TFT material systems, quantitative as well as qualitative differences in the response have been reported even for a given gate dielectric/AOS channel combination. TFT performance and stability can be sensitive to both channel and gate dielectric processing as well as to the details of the interface between them. Thus, some of the quantitative as well as qualitative differences in the gate bias stressing response may be attributed to processing differences (deposition method, annealing, etc.) and nonoptimized materials and interfaces. A few specific examples of the impact of 1) channel, 2) dielectric, and 3) interface processing on TFT stability are discussed. Also critical when interpreting results are ambient interaction and encapsulation (see Sections III-D and E).

a) AOS channel processing: Gorrn *et al.* [36] showed that, depending on the composition of their PA-PLD ZTO films, positive V_G bias stressing could produce either rigid positive V_T shifts or negative V_T shifts accompanied by S degradation. As shown in Fig. 11, they found out that a 36% Zn:64% Sn composition yielded optimum stability in the ALD

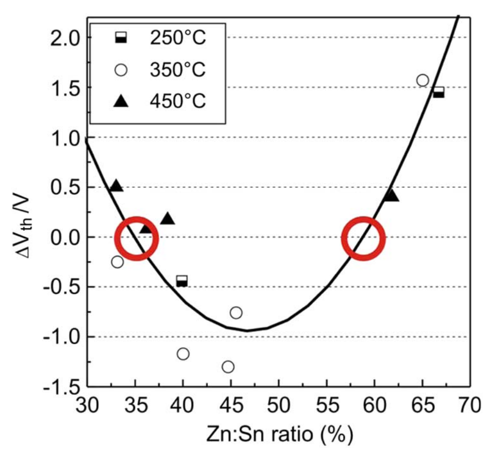

Fig. 11. Data from the study in [11]. Plot of the positive-gate-bias stress-induced ΔV_T versus the Zn:Sn ratio for the ALD ATO dielectric/ZTO channel TFTs.

ATO dielectric/ZTO channel TFTs [11]. Chiang *et al.* [60] reported that increasing the percentage of O_2 and decreasing the RF power during IGZO deposition increased the initial V_{ON} and improved the stability in thermal SiO_2 dielectric/RF-sputtered IGZO channel TFTs. Lim *et al.* [53] reported that the positive bias stress stability of ALD Al_2O_3 gate dielectric/ZnO:N channel SBG TFTs was improved with a higher N content.

Postdeposition annealing of the channel can also have an impact on trapping. As an example, Nomura *et al.* [40] found out that 400-°C postdeposition annealing in wet or dry O_2 reduced trapping in thermal SiO_2/PLD IGZO SBG TFTs, and Cho *et al.* [52] found out that a 4-h 200-°C anneal in air reduced V_T shifting in thermal SiO_2 gate/RF-sputtered IGZO SBG TFTs.

Jeong *et al.* [61] found out that the addition of Ga to solution deposited ZTO SBG TFTs improved the positive bias stress stability, which they attributed to a decrease in oxygen vacancies.

b) Gate dielectric processing: As might be expected, for a given dielectric material, deposition method and postprocessing have been reported to have an impact on bias stability. For example, Oh *et al.* [44] found out that bias instabilities due to RF-sputter damage of RF-sputtered Al_2O_3 gate dielectric ZnO TFTs were reduced when the RF-sputtered Al_2O_3 was densified by a postdeposition anneal and were nearly eliminated when ALD Al_2O_3 was used. Hoffman *et al.* found out that the ALD HfO_2 exhibited reduced V_T shifts compared to sputtered HfO_2 for IZO SBG TFTs [45].

c) Interface: The structure of the interface has also been demonstrated to have a major impact on device stability. Lee *et al.* [55] and Triska *et al.* [43] found out that the insertion of a thin interfacial layer between the gate dielectric and the channel can either degrade or improve the interface. Lee *et al.* reported that the insertion of a thin (~5 nm) interfacial layer of PECVD SiN_x between the 185-nm ALD Al_2O_3 top gate and the RF-sputtered IGZO channel resulted in a better saturation mobility, but a larger bias stress induced a V_T shift and increased S. Triska *et al.* found out that the insertion of a thin (~3 nm) PECVD SiO_x between the bottom 200-nm ALD Al_2O_3 gate dielectric and the RF-sputtered ZTO channel resulted in a reduced bias-stress-induced $+V_T$ shift, likely due to a reduced electron trapping.

7) Bias Stress Modeling and Mechanisms: The time dependence of the positive-bias-stress-induced positive V_T shift seen in many AOS TFT systems has been fit to both logarithmic and stretched exponential models.

A logarithmic dependence on stress time is indicative of trapping at pre-existing defects with a single (small) capture cross section, without the creation of new defects [62]. The logarithmic model was used to fit the time dependence of the bias-stress-induced V_T shift in RF-sputtered IGZO TFTs with a PECVD SiN_x gate dielectric and an SiO_x passivated IGZO surface [34] (Fig. 6), in RF-sputtered IGZO TFTs with a 5-nm interfacial PECVD SiN_x/ALD Al_2O_3 gate dielectric stack [55], in PLD IGZO TTFTs with an ALD ATO gate dielectric [39], and in RF-sputtered ZnO TFTs with a thermal SiO_2 gate dielectric [54]. Fujii *et al.* [34] also found out that recovery exhibited a logarithmic time dependence.

Many other groups have observed a stretched exponential time dependence for positive-bias-stress-induced positive V_T shift. The stretched exponential model can be expressed as

$$\Delta V_T = \Delta V_{T0}\left\{1 - \exp\left[-(t/\tau)^{\beta}\right]\right\} \quad (1)$$

where V_{T0} = saturation V_T, t = time, $\tau = \tau_0 \exp(E_\tau/kT)$, β = stretched exponent, E_τ = channel/dielectric average energy barrier, and $E_a = E_\tau \beta$ is the thermal activation energy.

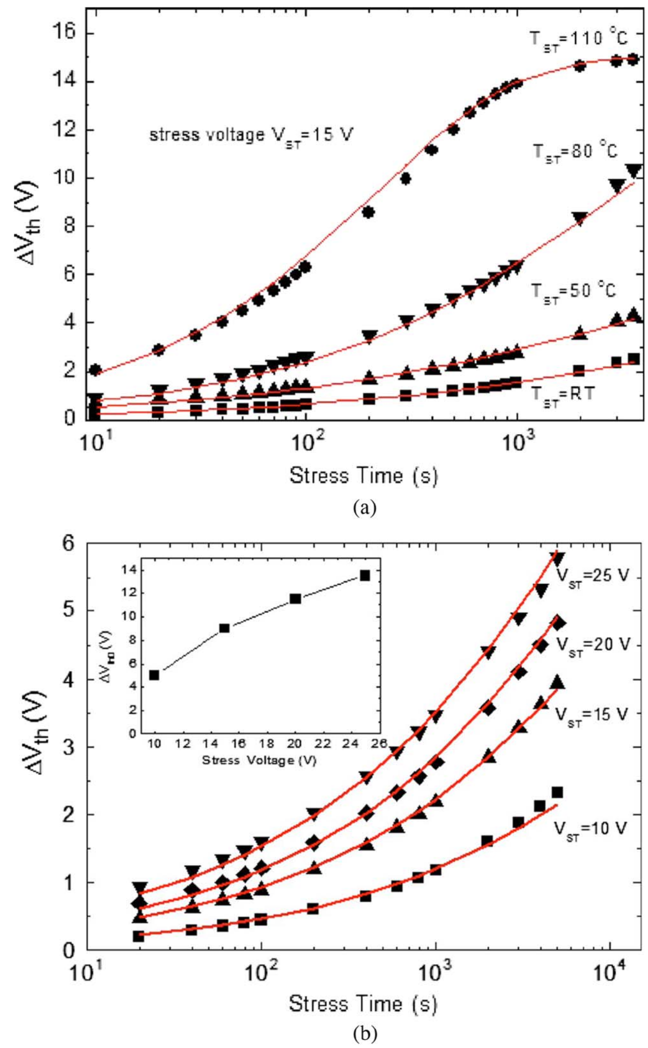

Fig. 12. Data from the study in [32]. Stretched exponential modeling of the positive-gate-bias-stress-induced $\Delta V_{\rm th}$ shift in RF-sputtered IGZO/thermally grown SiO_2 top gate TFTs as a function of the (a) temperature and (b) stress voltage.

It was first used to model trapping in a-Si:H systems by Libsch and Kanicki [63] and it has also been used to model charge trapping in high-κ dielectrics by Zafar *et al.* [64].

Lee *et al.* used stretched exponentials to fit the time dependence of the positive-bias-stress-induced V_T shift in RF-sputtered IGZO top gate TFTs with both thermally grown SiO_2 [32] (see Fig. 12) and ALD Al_2O_3 [55] gate dielectrics, and noted that the model could account for a variety of stress fields and temperatures. It is interesting to note that they saw a *logarithmic* fit versus time when a 5-nm SiN_x interfacial layer was inserted between the IGZO and Al_2O_3 [55], which they interpreted as an indication that the dielectric is the origin of the charge trapping and that charge is more easily redistributed in Al_2O_3. Nomura *et al.* [40] also used a stretched exponential to model positive-bias-stress-induced trapping in the PLD IGZO TFTs with thermal SiO_2 as a gate dielectric. However, contrary to Lee *et al.*, they suggested that the origin of the charge trapping was not in dielectric but either in the acceptor-like traps in the IGZO channel or at IGZO/SiO_2 interface.

Triska *et al.* [43] found out that, although a logarithmic model fits well the positive-gate-bias-induced V_{ON} shift for an RF-sputtered ZTO SBG TFT with an ALD Al_2O_3 gate dielectric, a stretched exponential model was required to fit the V_{ON} shift if the Al_2O_3 was capped with a thin ($\sim$2–5 nm) layer of PECVD SiO_2 or if the PECVD SiO_2 was used alone, indicating that the interface dominates the stress response.

Fung *et al.* [56] used a stretched exponential to model trapping in sputtered SiO_2 encapsulated IGZO channel SBG TFTs with RF-sputtered SiO_2 gate dielectrics. Good fit of the stretched exponential model to both positive and negative gate bias stressings for all stress temperatures was interpreted as carrier injection from the channel and subsequent charge trapping. The detailed fitting parameters suggested that there is a lower barrier for electron injection than for hole injection.

Lopes *et al.* [18] used a stretched exponential model to fit both positive V_T shift and *recovery* in unencapsulated RF-sputtered IGZO SBG TFTs with thermal SiO_2 gate dielectrics.

Cho *et al.* [52] found out that positive V_T shift and recovery in dynamically stressed thermal SiO_2 gate/RF-sputtered IGZO SBG TFTs were well modeled by stretched exponentials. The modeled recovery time constant was longer than the modeled stress time constant and was decreased with increasing temperature and V_{DS}. The authors concluded that the dominant mechanism was the trapping of the electrons in unstable traps at the interface or in the bulk with redistribution but negligible creation of additional interface traps. An incomplete recovery at room temperature suggested some deep trapping.

Shin *et al.* [57] used a modified stretched exponential to fit the *negative*-bias-stress-induced negative V_T shift in PE-ALD Al_2O_3/PE-ALD ZnO TTFTs that were simultaneously exposed to various intensities of 524-nm illumination.

Finally, Hoffman *et al.* [45] reported that stretched exponentials fit the positive-bias-stress-induced positive V_{ON} shift in ZIO channel SBG TFTs with either PECVD SiO_2 or PECVD SiN_x gate dielectrics.

Both the logarithmic and stretched exponential models have been interpreted as suggesting that charge trapping without the creation of new defects dominates the bias stress response [18], [30]–[32], [34], [39], [40], [43], [52], [56], [57]. The main difference between the physical interpretations of the two models is that, while the logarithmic model was developed based on the assumption of trapping at pre-existing defects with a single cross section, with no further redistribution of the charge after initial trapping [55], the stretched exponential model represented by (1) can be arrived at by assuming either 1) a redistribution of trapped charges at long stress times and large stress fields toward energetically deeper states in the bulk dielectric, where β relates to the energy barrier for charge distribution [63], or 2) the presence of a distribution of trap capture cross sections, where β relates to the width of distribution [64]. Note that without the benefit of additional information about point defects such as that provided by electron spin resonance (ESR), attaching a specific physical meaning to β is not straightforward.

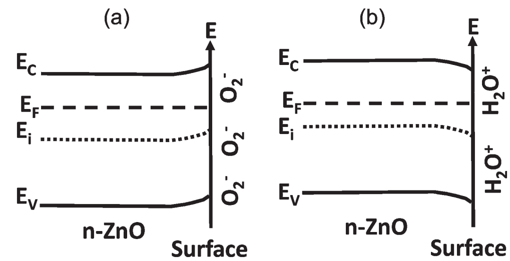

Fig. 13. Rough sketch showing the impact of (a) O_2^- and (b) H_2O^+ adsorption on band bending at an AOS surface.

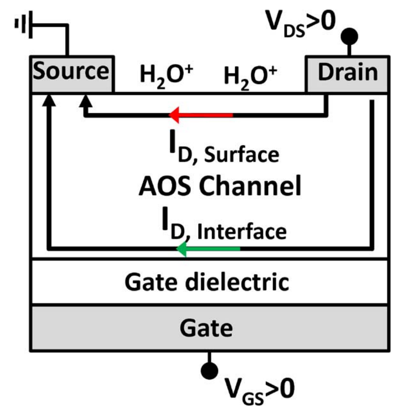

Fig. 14. Cross-sectional schematic of an unpassivated bottom gate TFT device illustrating the formation of a parasitic top gate channel due to surface adsorption [68].

C. Surface/Ambient Interaction

It is well known that metal oxides are surface sensitive to molecules in the ambient atmosphere [22]–[25]. For example, the adsorption of O_2 onto the surface of a metal oxide introduces an acceptor-like surface state: physisorbed O_2 is neutral when unoccupied and becomes chemisorbed and negatively charged $[O_2]^-$ when it captures (becomes occupied by) an electron from the CB. The resultant $[O_2]^-$ causes in surface depletion. Similarly, H_2O can act as a donor-like surface state (although the interaction of H_2O with the surface is more complex [25]). Other molecules such as H_2, CO_2, ethanol, etc., can also interact with metal oxide surfaces to produce changes in conductivity. Shown in Fig. 13 are rough sketches showing surface band bending and the generation of a surface depletion region as a result of chemisorbed $[O_2]^-$ [Fig. 13(a)] and formation of an accumulation region as a result of chemisorbed $[H_2O]^+$ [Fig. 13(b)] [65]–[67]. It can therefore be expected that when an SBG TFT channel is left unpassivated, as shown in Fig. 14 the surface-adsorbed H_2O or other donors may result in a parallel parasitic back channel conduction path [66]–[68]. Likewise, the removal of the adsorbed $[O_2]^-$ can also lead to increased surface carrier density and conductivity.

Vacuum desorption experiments on unpassivated bottom gate devices, with the channel surface exposed to ambient, illustrate the impact of the surface-adsorbed species. Kang *et al.* [69] looked at PECVD Si_3N_4/RF-sputtered IGZO channel SBG TFTs, while Gorrn *et al.* [70] investigated ALD ATO/PA-PLD ZTO SBG TFTs. Both of these studies reported that upon exposure to vacuum after storage in ambient unpassivated devices exhibited a negative V_T shift that is entirely reversible [69], [70]. Kang *et al.* further showed that postvacuum exposure to O_2 resulted in a super recovery of V_T, in which V_T overshoots the pre-exposure value to become more positive. Both groups concluded that the V_T shift appears to be dominated by O_2 desorption, but that H_2O also plays a role.

In a different type of study, PECVD Si_3N_4 dielectric/RF-sputtered IGZO SBG TFTs were soaked in DI H_2O and were then heated in vacuum, after which Park *et al.* [67] observed a positive shift, consistent with desorption of H_2O.

Ye *et al.* [71] found out that the mobility and carrier density of ZnO:N SBG TFTs both deteriorated after several weeks in atmosphere at 50 °C. Annealing at 400 °C in N_2 was found to improve shelf life. They tentatively attributed the degradation to the catalyzed hydrolyzation due to the adsorbtion of water and pollutants.

Finally, Gorrn *et al.* [70] demonstrated that surface O_2 interaction dominated the recovery response and so-called persistent photoconductivity in unencapsulated ZTO TFTs.

When taken together, these studies indicate that the surface interactions with the ambient must be considered when interpreting bias stressing and illumination studies of the unpassivated devices. Regarding illumination, it is well known that exposure to high-energy photons can result in the desorption of species from metal oxide surfaces. After the exposure is stopped, these species can take many minutes to reabsorb on the surface [22]–[25], [72]. As discussed in Section III-E, proper passivation or encapsulation of the channel surface can reduce or eliminate some ambient, bias stress, and illumination-induced instabilities by eliminating interaction with surface species.

D. Impact of Ambient on Bias Stressing

The results discussed in the last section demonstrate that surface/ambient interactions can impact the stability of the unbiased unencapsulated SBG TFTs. With reference to simple equations for gas molecule adsorption (e.g., $O_2(\text{gas}) + e^- \rightarrow O_2^-(\text{ads})$), Jeong *et al.* [65] discuss how positive bias stressing can lead to field-induced adsorption of O_2 and desorption of H_2O. ZnO nanowire sensor studies have also shown that gate bias can modulate gas sensitivity [72], [73]. In this section, recent results investigating the impact of ambient on bias stressing of unencapsulated SBG TFTs are discussed.

Lopes *et al.* [18] report that exposure of unencapsulated 40-nm RF-sputtered IGZO SBG TFTs with 100-nm thermal SiO_2 dielectrics to water vapor for 24 h resulted in an accelerated V_T shift upon subsequent bias stressing as compared to unexposed samples.

Liu *et al.* [38] found out that the stability of 50-nm RF-magnetron-sputtered IZO coplanar bottom gate TFTs with 300-nm Si_3N_4 gate dielectrics is degraded (larger V_T shifts) when low-field positive and negative bias stressings are conducted in ambient rather than in vacuum. The authors attributed the enhanced degradation to interaction of O_2 and H_2O at the channel surface.

Finally, as shown in Fig. 15, Lee *et al.* [10] found out that the negative-bias-stress-induced negative V_T shifts in unpassivated

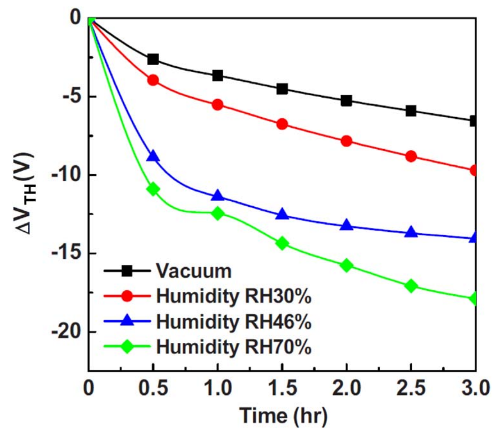

Fig. 15. Data from the study in [10]. Plot of ΔV_{th} versus time for the unpassivated SiN_x dielectric/IGZO SBG TFTs exposed to negative gate bias stress as a function of the relative humidity.

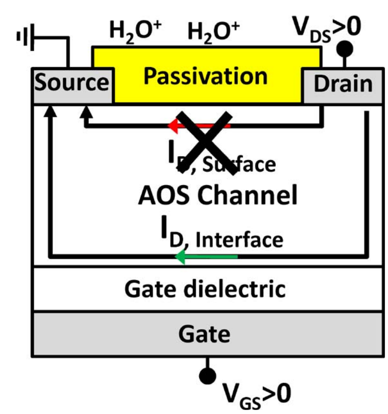

Fig. 16. Cross-sectional schematic of the passivated bottom gate TFT device illustrating the elimination of a potential parasitic top gate channel [68].

IGZO SBG TFTs with SiN_x dielectrics were progressively worse for increasing relative humidity levels from 0% to 70% humidity.

The work reviewed in this section demonstrates that ambient can have a profound impact on SBG TFT performance and stability under bias stressing and illumination. Moisture, in particular, has typically been observed to accelerate bias-stress-induced parametric shifts. It is very likely that the uncontrolled interaction of the unpassivated devices with the ambient can explain some of the differences in the illumination, bias stress, and recovery response reviewed in Section III-A and B. These results indicate that the passivation of the channel surface will likely have to be considered for the commercial applications of SBG TFTs. The effect of passivation of SBG TFTs is discussed in the next section. Note that top gate TFTs would not be expected to exhibit the same sensitivity, as they are essentially self-passivated.

E. Passivation/Encapsulation and Bias Stressing

As shown in Fig. 16, passivation or encapsulation of the AOS channel can physically prevent or kinetically inhibit [52] ambient molecules from adsorbing on AOS channel surface.

Many groups have shown that proper surface passivation can reduce or eliminate V_G stressing instabilities in bottom gate

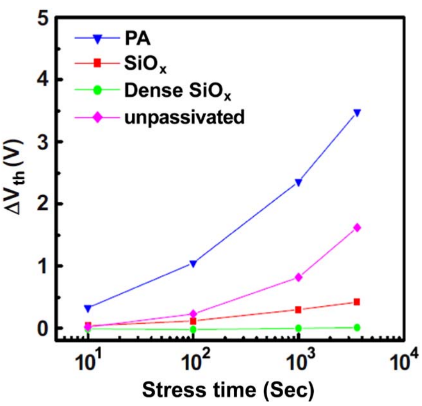

Fig. 17. Data from the study in [65]. Plot of the positive-gate-bias-stress-induced $\Delta V_{\rm th}$ versus time for the SiN_x/RF-sputtered IGZO SBG TFTs as a function of the channel passivation.

devices. As shown in Fig. 17, Jeong *et al.* [65] compared RF-sputtered IGZO passivated with either organic photoacryl (PA), PECVD SiO_x, or densified SiO_x with unpassivated IGZO TFTs and found out that while undensified SiO_x reduced and densified SiO_x nearly eliminated the V_T shift during positive V_G stressing, the PA passivated TFTs exhibited a degraded stability. Levy *et al.* [74] showed that 30-nm ALD Al_2O_3 passivated ALD ZnO TFTs exhibited much less $+V_G$ stress-induced V_T shift than the unpassivated devices. Many other groups have also reported dc bias stress stability improvements resulting from the passivation of a variety of AOS channel SBG TFTs including following: passivation of ZTO with a novel ALD Al_2O_3/ZrO_2 laminate [70], polyimide passivation of AZTO [75], 25-nm ALD Al_2O_3 encapsulation of Al/Sn doped ZIO [76], passivation of ZTO with a spin on SiO_x and PMMA [77], and passivation of PE-ALD ZnO with ALD Al_2O_3 [48], [49]. Seo *et al.* found out that TiO_x passivation of IGZO SBG TFTs improved both negative bias stress stability and environmental stability/aging [58]. Arai *et al.* [14] found out that dc-sputtered Al_2O_3 passivation of IGZO SBG TFTs performed better than either RF-sputtered SiO_x or CVD SiN_x/SiO_x passivation, whereas straight CVD SiN_x passivation actually degraded performance.

Cho *et al.* [52] reported a reduced V_T shift in dynamically stressed RF-sputtered IGZO SBG TFTs passivated with 100-nm RF-sputtered Al_2O_3.

Lee *et al.* [10] reported that a humidity-enhanced degradation during negative bias stressing was greatly reduced by 200-nm SiO_x passivation of their SiN_x/IGZO SBG TFTs.

Sato *et al.* [47] found out that PECVD SiO_x/Si_3N_4 (50/300 nm) surface passivated IGZO channel coplanar homojunction bottom PECVD SiO_x gate TFTs that were subjected to an environmental test for 116 h at 85 °C and 85% relative humidity showed only an ∼0.1-V V_T shift, indicating that the passivation layer protects the device (Other groups [18] have reported a negative V_T shift after exposure to humidity.).

Finally, Oh *et al.* [44] saw that for ALD Al_2O_3/RF-sputtered ZnO TFTs, use of *top gate* structure resulted in less positive-bias-stress-induced degradation than a bottom gate structure, even when the top gate structure was stressed at a 70% higher field.

Passivation can have unwanted side effects as well. For example, passivation has been reported to impact base device parameters for unstressed devices. Several groups have reported that passivated devices exhibit a negatively shifted V_T as compared to unpassivated devices, with no change in S or μ, including Gorrn *et al.* [70] (ALD Al_2O_3/ZrO_2 laminate passivated ZTO), Levy *et al.* [78] (ALD Al_2O_3 passivated ZnO), and Hong and Wager [68] (SiO_x, CaF, GeO_x, SrF, and SbO_x passivation of ZTO). This negative V_T shift is thought to be due to O_2 removal from the surface, leading to generation of higher carrier densities. Hong *et al.* [68] reported that NiO_x passivation of ZTO reduced peak mobility. Zhao *et al.* [48] and Mourey *et al.* [49] reported that ALD Al_2O_3 passivation of PE-ALD Al_2O_3/PE-ALD ZnO resulted in an ∼2-V shift in V_T and an increased S but with a reduced hysteresis. In another work, the spin coat polyimide passivation of AZTO improved S [76].

In summary, it is clear from the work discussed in this section that passivation can play a major role in TFT performance and stability. In order to be effective, the passivating layer must be compatible with the underlying channel layer, must be thick enough to eliminate the influence of surface-adsorbed species, must be a good enough diffusion barrier to eliminate the diffusion of surface species to the passivating layer/channel interface, and should have a low hydrogen content [13], [68]. Proper passivation can reduce or eliminate surface- and bias-stress-induced instabilities in bottom gate devices without impacting the base device parameters. A careful passivation is thought to be critical in producing stable SBT TFTs for commercial applications [12]–[14]. Passivation is not as much of a concern for top gate devices which are self-passivated by the overlying gate dielectric.

F. Mechanical Stress

For flexible circuit applications, it is important to know the impact of mechanical strain and flexing on TFT stability. Nomura *et al.* [7] looked at the impact of bending-induced tensile stress on unencapsulated 140-nm PLD Y_2O_3 dielectric/30-nm PLD IGZO SBG TTFTs and found out that the application of 0.3% tensile strain resulted in a slight decrease in saturation current, but that the devices were stable when subjected to repetitive bending.

G. Defects

A fundamental understanding of the structure and nature of point defects that are responsible for electrically induced instabilities is often necessary in fully optimizing the material and device performance. Electron paramagnetic resonance (EPR), also known as ESR, is the only technique that can provide detailed structural information about electrically active point detects [79]. EPR studies have identified dominant electrically active defects in both Si/SiO_2 and a-Si:H/Si_3N_4 systems.

For Si/SiO_2 system, EPR studies have shown that two types of Si dangling bond centers dominate the performance and reliability of MOS devices: P_b centers ($Si_3 \equiv$ Si•) at the Si/SiO_2 interface and E' centers ($O_3 \equiv$ Si•) in the SiO_2 [79]–[81]. For the a-Si:H/Si_3N_4 system, EPR studies have also shown that the silicon dangling bond centers are dominant: D-centers

($Si_3 \equiv Si\bullet$) in the a-Si:H [82] are created by illumination [2] and bias stressing [1], and K centers ($N_3 \equiv Si\bullet$) are populated by charge injection into the Si_3N_4 [83]. The understanding of these defects has allowed both of these technologies to flourish.

EPR investigations have also begun to shed light on electrically active and stress-induced defects in thin-film high-κ dielectrics [84]. In bulk ZnO powder, EPR studies have shown that oxygen vacancies are likely responsible for the green luminesence [85]. Very recently, Jeong *et al.* [61] observed an EPR resonance with a Landé g-factor equal to 1.9559 in solution-deposited Ga doped and undoped ZTO films, which they tentatively assigned to oxygen vacancies (V_O). They also reported that the 40% lower spin density that they saw in Ga doped ZTO was accompanied by a reduction in the bias-stress-induced V_T shift, suggesting that this defect may play a role in the bias stress stability of these devices. With the exception of the study in [61], there have been no dedicated EPR investigations performed on thin-film AOS materials and no consideration of any of the many combinations of high-κ dielectric/AOS channel interfaces that are being used to make TFTs.

Although groups have begun to map the subgap density of states in IGZO [21], [86], [87] and ZTO [26], which is useful in understanding device performance and mobility, the identification of the defect structures that are responsible for instabilities in AOS TFTs remains a wide open field. To date, there is no direct experimental evidence linking specific defect structures to bias-stress-induced instabilities. Much work needs to be done to understand the nature of the defects in the AOS materials, in high-κ dielectrics, and especially at AOS/dielectric interface in the AOS TFTs.

IV. Summary/Conclusion

Novel AOS TFT channel materials such as ZTO, IGZO, ZITO, etc., exhibit several advantages over a-Si:H TFTs, such as mobility in the range of $\sim$5–> 50 $cm^2/V \cdot s$, low temperature processing, and transparency in the visible portion of the spectrum [6]. An obvious application of these materials is transparent electronics. Although it will be difficult to displace a-Si:H, especially for large-area displays, another potential application for AOS TFTs is as backplanes for high-performance AMLCDs. Probably the most likely target application for these new materials is using them as an AM-TFT backplane for the emerging OLED display technology. For the first two applications, TFTs need to remain stable while operating under continuous exposure to illumination. Because OLED displays are emissive and current driven, TFT stability is critical as any shift in V_T would result in a change in pixel brightness [6], [11], [15]–[18]. V_T stability under a gate bias stress is recognized as one of the most significant issues in commercializing AOS TFT technology for AMOLED displays [13], [14].

Despite its importance, investigation of AOS TFT stability is still an emerging area. The first TTFTs were reported in 2003. The first paper on ZnO TFT stability under bias stressing was published in 2006 [30]. Since then, the number of stability-related AOS TFT papers has roughly doubled each year. A number of potential reliability problems have been identified and have begun to be investigated in a number of combinations of AOS channels and gate dielectrics. Direct comparisons of the studies to date are difficult due to the details of the materials, device structure, and stress conditions, and there have been a few extensive systematic studies. Nevertheless, some general trends can be identified with respect to stability under the following: 1) illumination; 2) bias stress; and 3) channel surface/ambient interaction.

Illumination: although a-Si:H devices exhibit well-known instabilities upon exposure to visible illumination that results in permanent changes, the AOS materials, in general, exhibit little sensitivity to ambient lighting, reversible changes as the photon energy approaches the bandgap, and no permanent changes even upon exposure to high-energy illumination [27]–[29]. Sensitivity to illumination can be minimized by encapsulation and by using UV absorbing coatings which would not impact applications requiring transparency in the visible part of the spectrum [27].

Bias stressing: bias stressing of the a-Si:H/Si_3N_4 TFTs results in defect creation in the channel and charge trapping gate dielectric or at channel/dielectric interface that is irreversible without annealing. AOS TFTs have also been found to be sensitive to bias stressing. In contrast to a-Si:H, the majority of the AOS TFT studies to date suggest that instability problems due to low-field positive gate bias stress can be explained by trapping and detrapping at pre-existing defects at or near dielectric/channel interface, with little creation of new defects, and rapid recovery without annealing [18], [30]–[49], [52], [53]. This general result is consistent with the suggestion that the nature of bonding in AOS materials (e.g., carrier conduction through metal ns orbitals instead of covalent sp^3 orbitals [7]) affords them a greater resistance to defect and dangling bond formation than a-Si:H [8], [9]. Defect creation and recovery that requires annealing have been reported in some studies of high-field (> 1 MV/cm) stressing [30], [54], [55], and they are topics that require more investigation.

Ambient interaction: the majority of the AOS TFTs investigated to date are SBG devices without passivation, in which the AOS channel surface is left exposed to ambient. The surface sensitivity of metal oxides is well known. For example, adsorption and desorption of molecules from ambients such as O_2, H_2O, etc., can result in the accumulation or depletion of the surface region and can affect the conductivity and performance of the device [65]–[70]. Thus, the impact of surface interactions on the unpassivated devices cannot be ignored when interpreting bias stress results. Indeed, channel surface/ambient interaction has recently been demonstrated to have a significant impact on both bias and illumination stressing of the SBG TFTs [10], [18], [41]. As surface effects were not fully taken into consideration in many of the early studies, in addition to the obvious importance of processing, they might explain a large part of the discrepancies reported between different studies for otherwise similar material systems. Fortunately, the surface-induced instabilities in the SBG TFTs can be reduced or eliminated either by a proper passivation of top and back-channel surface of the AOS channel or by a top-gate device structure in which the gate oxide self-passivates the AOS channel [10], [44]–[49], [52], [65], [68], [70]–[77].

Given this general summary of what is known so far, what are the challenges in improving the stability and reliability of the AOS TFTs for commercial applications? I believe that the main challenges include the following: 1) finding the right dielectric for a given channel material; 2) proper passivation; 3) application-directed characterization; and 4) defect identification.

Materials and the AOS/dielectric interface: it is well known that the interface between a channel material and the dielectric can have a large impact on field-effect transistor operation and stability. Just as Si_3N_4 has allowed a:SiH to enjoy a huge commercial success, the identification of the best dielectric for each AOS channel material such as IGZO and ZTO is needed to allow these materials to reach their full commercial potential. Although much of the work to date has used thermally grown SiO_2 as a bottom gate dielectric, thermally grown SiO_2 is not compatible with transparent applications. More work is needed in which high-κ dielectric materials deposited by various methods are systematically compared on the same channel in order to identify the most promising dielectric/AOS channel combinations [43], [45], [46], [51]. Once promising combinations have been identified, process optimization can target further improvements in stability.

Passivation: it has been recently demonstrated that proper passivation of the AOS channel surface can eliminate the influence of ambient and, in some cases, can improve bias stability. However, other work has shown that improper passivation does not prevent surface interaction or can have unwanted side effects such as V_T shift and reduced mobility [48], [49], [68], [70], [78]. A suitable passivation layer should eliminate the effect of ambient interaction without deleteriously affecting device operation. Without proper passivation, stability results on a given device cannot be viewed as conclusive, and it is now widely agreed that passivation is critical for commercial AOS TFT applications [12]–[14]. Much work still needs to be done to identify the passivation layers that are suitable for a given AOS material. As the case for gate dielectrics, it is unlikely that a single material can serve as a suitable passivation layer for all channel materials.

Application-directed characterization: so far, the majority of the work investigating the stability of the AOS TFTs has been on single devices subjected to a single type of stress. Although this is necessary and very useful, with the strong drive toward commercialization, the next step is to assess stability and reliability under projected use conditions. Several questions need to be answered about appropriate stress conditions, multiple stressing, recovery, and mitigation. For example, for a given AOS/dielectric TFT combination, is single device bias stressing too harsh or too conservative? If one wishes to save time and perform accelerated stress at elevated fields, will the damage mechanisms remain the same? Does exposure of a device simultaneously to multiple types of stress lead to unanticipated interactions? Switching TFTs in AMLCDs will be subjected to continuous illumination from the backlight. It has very recently been shown that simulated backlight illumination exacerbates the negative-bias-stress-induced V_T shift [10], [57]. Much more work needs to be done to test passivated devices under simultaneous bias stressing and illumination. However, another issue is the widely reported rapid recovery of V_T shift in unbiased devices at room temperature. This recovery contributes to a complex time dependence that will have to be well understood and modeled for circuit applications. As an example, it has been shown that due to the effects of recovery, V_T shift is a function of stress frequency—higher frequency dynamic stressing results in less damage than static stressing [52], [59]. Finally, is parametric drift a problem for the intended application, or can some level of device deterioration be tolerated or mitigated? Recent work has shown that active mitigation such as V_T compensation circuitry can be used for some AOS devices [13].

Defects: knowledge of the structure of the defects that are responsible for the instabilities can greatly aid in the reduction of these defects and in the optimization of performance and stability. For example, a strong understanding of defects at Si/SiO_2 interface helped in enabling the MOS technology to become the dominant microelectronics technology. Likewise, an understanding of the a-Si:H/Si_3N_4 interface enabled this technology to dominate TFT applications. It is likely that an equivalent basic understanding of the defects that are responsible for instabilities in AOS TFTs for specific AOS/gate dielectric systems will be critical before the commercial application in OLED displays or other areas such as flexible electronics can be realized. This area, in particular, is ripe for more work.

In conclusion, initial reports suggest that AOS TFTs exhibit promising stability compared to a-Si:H with respect to illumination and bias stressing. If these instabilities can be fully understood and minimized, AOS technology has a bright future.

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